BENTIAN JIANG

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PROFESSIONAL SUMMARY

I am a Principal Engineer and Team Lead at the EDA Lab in Huawei Hong Kong Research Center, leading a team of 4-5 engineers in developing PPA-driven arithmetic optimization engine for physical/3D-aware RTL compiler. I hold a Ph.D. from CUHK (2021, Advisor: Prof. Evangeline F.Y. Young) and a B.Eng. from Sichuan University.

My work bridges theoretical algorithms with industrial applications, featuring extensive experience in developing & deploying proprietary synthesis tools for top-tier domestic NPU, CPU, GPU, DSP, and Modem chips in China. My dedicated team focuses on PPA-driven computer arithmetic implementation and optimization engine (including MAC, ALU, FPU, additions, division/modulo and etc.) for the most internally critical and high-performance designs. I am a recipient of the company's Individual Golden Medal Award (Top 1%).

Career Objective: I am looking to pivot my extensive compiler and datapath expertise into AI-driven domains. Specifically, I aim to (1) advance Agentic Design Automation for AI chip design; (2) break the boundary between RTL compilation and micro-arch design or (3) contribute to high-performance AI Compiler/Infrastructure stacks.

Location Preference: Hong Kong SAR (eligible for HK PR; no visa sponsorship required)

EDUCATION

The Chinese University of Hong Kong, Hong Kong SAR Aug. 2017 – July 2021
Ph.D., Department of Computer Science & Engineering
Dissertation: "Towards Automated End-to-end VLSI Design for Manufacturability Solutions"
Advisor: Prof. Evangeline F.Y. Young (CSRankings: CUHK CSE ranked **1st** in the field of Design Automation)

Sichuan University, P.R. China Sep. 2013 – Jul. 2017
B.Eng., Electronic & Information Engineering

PROFESSIONAL EXPERIENCE

Principal Engineer | Huawei Hong Kong Research Center Sept. 2021 – Present, Hong Kong SAR

- RTL Compiler, Computer Arithmetic (Datapath)

* Awardee of *Individual Golden Medal Award* (Highest individual award, Top 1%)

Software Engineer Intern | Cadence Design Systems Inc. April 2019 – Sept. 2019, Austin, TX, USA

- Innovus Clock Tree Synthesis Team, 3 asscoiated US patents

SELECTED PROJECTS

Computer Arithmetic Optimization Engine in RTL Compiler

[*] Lead Architect of a proprietary RTL compiler's datapath optimization engine. Directed a 5-person team to build the engine from scratch, implementing novel compiler techniques, algorithmic innovations and deep in-house customization that delivered superior PPA metrics over commercial alternatives. Demonstrated silicon-proven success across (full-chip) Modem and (partial critical hardens) CPU/NPU tapeouts. Possess deep domain expertise in computer arithmetic design, spanning from micro-architecture to standard cell levels.

AI & Scientific Workloads Compilation on Dataflow Chip

[*] Led a team to win the Championship at the (Cerebras-held) ISPD 2019 Contest by architecting a DNN workload mapping and optimization framework that generates optimal execution plans for the Cerebras WSE (the world's largest dataflow chip).

[*] Secured 2nd Place at the ISPD 2020 Contest by developing a specialized workload compiler tailored for solving 3D partial differential equations (PDEs) in Finite Element models on the Cerebras WSE architecture.

PATENTS & PUBLICATIONS

Summary

US patents (3), IEEE TCAD (CCF-A, 5), DAC (CCF-A, 4), ACM TODAES (CCF-B, 1), ICCAD (CCF-B, 3), ASP-DAC (CCF-C, 2), ISPD (CCF-C, 1).

Patents

[P3] **Bentian Jiang**, Natarajan Viswanathan, Zhuo Li, Yi-Xiao Ding, "Machine-learning based clustering for clock tree synthesis." U.S. Patent 11,645,441, issued May 089, 2023..

[P2] **Bentian Jiang**, Natarajan Viswanathan, Zhuo Li and Yi-Xiao Ding, "Machine-learning based prediction method for iterative clustering during clock tree synthesis." U.S. Patent 11,244,099, issued Feb 08, 2022..

[P1] **Bentian Jiang**, Natarajan Viswanathan, William Robert Reece, and Zhuo Li. ''Dynamic weighting scheme for local cluster refinement." U.S. Patent 11,188,702, issued Nov 30, 2021.

Journal Papers

[J6] Zepeng Li, Zhen Zhuang, Genggeng Liu, **Bentian Jiang**, Weihua Sheng, Tsung-Yi Ho, "Redistribution Layer Routing for Fan-Out Wafer-Level Packaging Considering Multiple Advanced Design Rules", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J5] Tianji Liu, Nutdranai Jaruthikorn, Shiju Lin, **Bentian Jiang**, Guannan Guo, Weihua Sheng, Evangeline FY Young, ''Efficient and Effective E-graph-based Logic Optimization", ACM Transactions on Design Automation of Electronic Systems (**TODAES**), Volume 31, Issue 2, Article No.: 22, December 2025.

[J4] Lixin Liu, Tianji Liu, **Bentian Jiang**, Evangeline FY Young, "Parmesan: Efficient Partitioning and Mapping Flow for DNN Training on General Device Topology", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), Volume: 43, Issue: 8, August 2024..

[J3] **Bentian Jiang**, Xinshi Zang, Martin D.F. Wong and Evangeline F.Y. Young, "Exploring Rule-free Layout Decomposition via Deep Reinforcement Learning", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), Volume: 42, Issue: 9, September 2023.

[J2] **Bentian Jiang**, Lixin Liu, Yuzhe Ma, Bei Yu and Evangeline F.Y. Young, "Neural-ILT 2.0: Migrating ILT to Domain-specific and Multi-task-enabled Neural Network", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), Volume: 41, Issue: 8, August 2022.

[J1] **Bentian Jiang***, Jingsong Chen*, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang and Evangeline F.Y. Young, "CU.POKer: Placing DNNs on WSE with Optimal Kernel Sizing and Efficient Protocol Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), Volume: 41, Issue: 6, June 2022.

Conference Proceedings

[C10] Shiju Lin, **Bentian Jiang**, Weihua Sheng and Evangeline Young, "Size-Optimized Depth-Constrained Large Parallel Prefix Circuits", ACM/IEEE Design Automation Conference (**DAC**, CCF-A, top conference in EDA), San Francisco, CA, USA, June 23-27, 2024.

[C9] Qijing Wang, **Bentian Jiang**, Martin D.F. Wong and Evangeline F.Y. Young, "A2-ILT: GPU Accelerated ILT with Spatial Attention Mechanism", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, USA, Jul. 10-14, 2022.

[C8] Jinwei Liu, Xiaopeng Zhang, Shiju Lin, Xinshi Zang, Jingsong Chen, **Bentian Jiang**, Martin D.F. Wong and Evangeline F.Y. Young, "Partition and Place Finite Element Model on Wafer Scale Engine", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, Jul. 10-14, 2022.

[C7] **Bentian Jiang**, Xiaopeng Zhang, Lixin Liu and Evangeline F.Y. Young, "Building up End-to-end Mask Optimization Framework with Self-training", ACM International Symposium on Physical Design (**ISPD**), Virtual Conference, March 21-24, 2021.

[C6] **Bentian Jiang**, Lixin Liu, Yuzhe Ma, Hang Zhang, Bei Yu and Evangeline F.Y. Young, "Neural-ILT: Migrating ILT to Neural Networks for Mask Printability and Complexity Co-optimization, The 39th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), San Diego, CA, USA, Nov. 2-5, 2020.

[C5] **Bentian Jiang***, Jingsong Chen*, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang, Evangeline F.Y. Young, "CU.POKer: Placing DNNs on Wafer-Scale AI Accelerator with Optimal Kernel Sizing", The 39th

IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), San Diego, CA, USA, Nov. 2-5, 2020 (* indicates co-first authors).

[C4] Haocheng Li, Gengjie Chen, **Bentian Jiang**, Jingsong Chen, and Evangeline F.Y. Young, "Dr. CU 2.0: A Scalable Detailed Routing Framework with Correct-by-Construction Design Rule Satisfaction", The 38th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Westminster, CO, USA, Nov. 4-7, 2019.

[C3] **Bentian Jiang**, Xiaopeng Zhang, Ran Chen, Gengjie Chen, Peishan Tu, Evangeline F.Y. Young and Bei Yu, "FIT: Fill Insertion Considering Timing", The 57th ACM/IEEE Design Automation Conference (**DAC**), Las Vegas, NV, USA, June 2-6, 2019.

[C2] Gengjie Chen, Chak-Wa Pui, Haocheng Li, Jingsong Chen, **Bentian Jiang**, Evangeline F.Y. Young, "Dr. CU: Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search", IEEE/ACM Asia and South Pacific Design Automation Conference (**ASP-DAC**), Tokyo, Japan, Jan 21-24, 2019.

[C1] **Bentian Jiang**, Hang Zhang, Jinglei Yang and Evangeline F.Y. Young, "A Fast Machine Learning-based Mask Printability Predictor for OPC Acceleration", IEEE/ACM Asia and South Pacific Design Automation Conference (**ASP-DAC**), Tokyo, Japan, Jan 21-24, 2019.

SELECTED AWARDS AND HONORS

Individual Golden Medal Award (**Top 1%**, 4 out of 400+)	Huawei Tech.	2023
The Hong Kong, China - Asia-Pacific Economic Cooperation Scholarship	HKSAR	2021
Talent Development Scholarship	HKSAR GSF	2021
DAC Young Fellow Award	DAC	2020
Championship at Contest on Wafer-Scale Deep Learning Accelerator Placement (Leader)	ISPD (Cerebras)	2020
Championship at Contest on Initial Detailed Routing	ISPD (Cadence)	2019
2nd Place Award at Contest on Timing-aware Dummy Fill Insertion (Leader)	ICCAD (Synopsys)	2018
2nd Place Award at Contest on Initial Detailed Routing	ISPD (Cadence)	2018
Full Postgraduate Studentship	CUHK	2017-2021
Outstanding Graduate	SCU	2017

PROFESSIONAL SERVICES

Technical Program Committee Member

- IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B), 2022

Journal Reviewer

- ACM Transaction on Design Automation of Electronic Systems (**TODAES**, CCF-B)
- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**, CCF-A)
- Integration, the VLSI Journal

Conference Reviewer

- ACM/IEEE Design Automation Conference (**DAC**, CCF-A)
- IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**, CCF-B)
- IEEE/ACM Asia and South Pacific Design Automation Conference (**ASP-DAC**, CCF-C)
- ACM International Symposium on Physical Design (**ISPD**, CCF-C)

TECHNICAL SKILLS

Domain Expertise	RTL/Verilog Compiler, Computer Arithmetic (Datapath), E-graph Optimization, Logic Optimization, Dataflow AI Workload Compiler
Languages	C/C++, Python, Tcl, LaTeX
Tools	Synopsys Design Compiler, Synopsys PTPX, Cadence Innovus